What Is Claimed Is:

1. An error detecting circuit comprising:

an error data storing unit for dividing a circuit implemented in a chip into predetermined areas, and outputting a plurality of error signals in response to a plurality of state error signals, a serial chain signal, a lock-enable signal, and a chip error signal, each of the plurality of state error signals being enabled when an error occurs in a corresponding predetermined area, the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit, and the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals output from the error data storing unit,

wherein the error data storing unit stores and outputs at least one of the plurality of state error signals and, in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit.

2. The error detecting circuit of claim 1, wherein the error data storing unit comprises a plurality of error data registers, each of the plurality of error data registers comprising:

a first error data register for outputting a first error signal in response to a first state error signal, the serial chain signal, the lock-enable signal and the chip error signal;

second through (N-1)-th error data registers for respectively outputting second through (N-1)-th error signals in response to second through (N-1)-th state error signals, the serial chain signal, the lock-enable signal, the chip error signal, and the first error signal; and

an N-th error data register for outputting an N-th error signal in response to an N-th state error signal, the serial chain signal, the lock-enable signal, the chip error signal, and the (N-1)-th error signal, wherein the first state error signal, the second through (N-1)-th state error signals, and the N-th state error signal are comprised in the plurality of state error signals.

3. The error detecting circuit of claim 2, wherein the first error data register comprises:

a NAND gate for outputting a control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the first error signal or the first state error signal in response to the serial chain signal and the control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the first error signal.

4. The error detecting circuit of claim 3, wherein the output terminal of the D flip-flop is a positive output terminal.

5. The error detecting circuit of claim 2, wherein any one of the second through (N-1)-th error data registers comprises:

a NAND gate for outputting a control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the first error signal, the second error signal and the second state error signal, in response to the serial chain signal and the control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the second error signal.

6. The error detecting circuit of claim 5, wherein the output terminal of the D flip-flop is a positive output terminal.

7. The error detecting circuit of claim 2, wherein the N-th error data register comprises:

a NAND gate for outputting an N-th control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the (N-1)-th error signal, the N-th error signal and the N-th state error signal in response to the serial chain signal and the N-th control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the N-th error signal.

8. The error detecting circuit of claim 5, wherein the output terminal of the D flip-flop is a positive output terminal.

9. A device for detecting an error in a circuit implemented in a chip, the device comprising

an error data storing unit for dividing the circuit into a plurality of predetermined areas and outputting a plurality of error signals in response to a plurality of state error signals, a serial chain signal, a lock-enable signal, and a chip error signal, each of the plurality of state error signals being enabled when an error occurs in a corresponding one of the plurality of predetermined areas, the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order, and the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals,

wherein the error data storing unit stores and outputs at least one of the plurality of state error signals to specifically indicate which of the predetermined areas contain the error.

10. The error detecting circuit of claim 9, wherein the error data storing unit outputs the at least one of the plurality of state error signals during a normal operation to retrieve error information.

11. The error detecting circuit of claim 9, wherein the error data storing unit outputs the at least one of the plurality of state error signals during an abnormal operation in which the chip goes out of order, in response to the serial chain signal.

12. The error detecting circuit of claim 11, wherein the serial chain signal is provided externally with respect to the chip.

13. The error detecting circuit of claim 9, wherein the error data storing unit comprises a plurality of error data registers, each of the plurality of error data registers comprising:

a first error data register for outputting a first error signal in response to a first state error signal, the serial chain signal, the lock-enable signal and the chip error signal;

second through (N-1)-th error data registers for respectively outputting second through (N-1)-th error signals in response to second through (N-1)-th state error signals, the serial chain signal, the lock-enable signal, the chip error signal, and the first error signal; and

an N-th error data register for outputting an N-th error signal in response to an N-th state error signal, the serial chain signal, the lock-enable signal, the chip error signal, and the (N-1)-th error signal, wherein the first state error signal, the second through (N-1)-th state error signals, and the N-th state error signal are comprised in the plurality of state error signals.

14. The error detecting circuit of claim 13, wherein the first error data register comprises:

a NAND gate for outputting a control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the first error signal or the first state error signal in response to the serial chain signal and the control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the first error signal.

15. The error detecting circuit of claim 14, wherein the output terminal of the D flip-flop is a positive output terminal.

16. The error detecting circuit of claim 13, wherein any one of the second through (N-1)-th error data registers comprises:

a NAND gate for outputting a control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the first error signal, the second error signal and the second state error signal, in response to the serial chain signal and the control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the second error signal.

17. The error detecting circuit of claim 16, wherein the output terminal of the D flip-flop is a positive output terminal.

18. The error detecting circuit of claim 13, wherein the N-th error data register comprises:

a NAND gate for outputting an N-th control signal in response to the lock-enable signal and the chip error signal;

a multiplexer for selecting one of the (N-1)-th error signal, the N-th error signal and the N-th state error signal in response to the serial chain signal and the N-th control signal; and

a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the N-th error signal.

19. The error detecting circuit of claim 18, wherein the output terminal of the D flip-flop is a positive output terminal.